APPLICATION NOTE

ABSTRACT
Due to the obsolescence of the PDI1394P11A physical layer device in December 2000, many designers may need to redesign their boards to incorporate a new physical layer device that is recommended for new designs. This document was written to inform these designers of Philips Semiconductors' redesign recommendations and to make this transition as easy as possible.

AN2455

Transitioning from the Philips Semiconductors PDI1394P11A to the PDI1394P2x family

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AN2455

1. INTRODUCTION

The PDI1394P11A 3-Port Physical Layer Interface chip was obsoleted in December 2000. The PDI1394P11A (will be referred to as the P11A throughout this document) was a 200 Mb/s device that was designed around the IEEE 1394-1995 standard, which has since been amended by the IEEE 1394a-2000 specification. This amendment was implemented to extend the usefulness of the 1394 Bus. Even though the purpose of this document is not to explain or compare the differences between the 1394-1995 standard and the 1394a-2000 standard, it is important to highlight the new features of the 1394a-2000 specification so the reader may obtain some insight as to which additions may be beneficial to their design. Section 2 briefly highlights these additions to the IEEE 1394a-2000 standard and attempts to clarify whether these additions require any firmware or hardware modifications to their existing P11A design.

The PDI1394P2x physical layer devices (referred to as P2x through out this document) are recommended replacements for the P11A. The P2x devices are not pin compatible to the P11A, so board layout changes must be made to incorporate the P2x into a current P11A design. For a complete listing of the P2x family see Table 1.

Table 1. PDI1394P2x family selection guide

Feature	PDI1394P21 & PDI1394P22	PDI1394P23 & PDI1394P24	PDI1394P25
Speed	400	400	400
No. Of Ports	3	2	1
IEEE1394-compliant	IEEE1394a-2000	IEEE1394a-2000	IEEE1394a-2000
Power supply	3.3 V (5 V tolerant I/O)	3.3 V (5 V tolerant I/O)	3.3 V (5 V tolerant I/O)
Supply current in power-down mode	150 μA	150 μA	150 μA
Additional features	P21 requires fewer external components than TI devices	P23 can be configured as a 1 port Phy with no extra external components	Requires fewer external components than TI devices
Availability	Samples – Now Production – Q3 ’01	Samples – Now Production – Q2 ’01 (P23) Production – Q3 ’01 (P24)	Samples – Now Production – Q2 ’01
Package	LQFP80 (P21) LQFP64 (P22)	LQFP64	LQFP64
Pin compatibility	TI TSB41LV03x/ TSB41AB3 – P21 Lucent (Agere) FW803 – P22	TI TSB41LV02x/ TSB41AB2 –P23 Lucent (Agere) FW802 – P24	TI TSB41LV01/ TSB41AB1* – P25

* 64-pin package.

2. NEW FEATURES OF IEEE 1394a-2000

The changes in the IEEE 1394a-2000 specification are incremental enhancements to the existing IEEE 1394-1995 standard. The P2x family is designed around the IEEE 1394a-2000 standard and incorporates all of the enhancements made to the standard. The P11A device was designed around the time when the IEEE 1394a-2000 standard was just evolving. Since some of the new enhancements being made to the IEEE 1394-1995 standard were known at this time, they were incorporated into the P11A. The enhancements that were implemented in the P11A are noted after their description.

- **Connection debounce**
  This was implemented for two main reasons:
  - The first being that the physical connection of the cables is not a smooth process. As the plug and connector scrape together, electrical contact is made and broken many times. This can create a storm of connects and disconnects that can extend the bus initialization well past the 200 μs (approximate time) that is normally takes.
  - When two nodes are connected together, it is unusual for the bias to be detected by both nodes at the same time. The node that first detects the bias will try to initiate a bus reset, but will be unable to complete the bus initialization until the other node detects the bias. When the other node detects this bias it will also initiate a bus reset. This process could interrupt operation of the bus for tens of milliseconds, which is undesirable.

  This improvement was implemented in the P11A. This is a silicon improvement and has no firmware implications.

- **Arbitrated (short) bus reset**
  This was defined to reduce the time the bus is unusable during bus initialization. During the initialization stage the following events occur, Bus Reset, Tree-ID, and Self-ID. The longest of these phases is in the Bus Reset, which lasts 167 μs. This time has to be longer than the nominal isochronous cycle time to insure that the bus reset is seen by every node, due to a transmitting node not being able to see the reset until it has finished transmitting.

  If the node initiating the bus reset arbitrates for the bus, then it is guaranteed that no other node is transmitting, which allows the node initiating the bus reset to send a shorter reset signal. This shortened signal is 1.3 μs long. For more information about bus reset actions and conditions, please see the IEEE 1394a-2000 standard, sections 3.9.2.1 and 4.4.3.1.

  This improvement was implemented in the P11A. This function is implemented by writing to a register called ISBR in the Phy (Physical Layer Chip). Please see the appropriate data sheet for further information.

- **Ack-accelerated arbitration**
  This allows arbitration to begin immediately after an acknowledge packet is observed.

- **Fly-by-concatenation**
  This is a method that can be used to eliminate delays during arbitration. When a transaction is being performed, a multi-port node must repeat the transaction on its other ports. If the packet being transmitted requires no acknowledge packet returned (i.e., acknowledge packets and isochronous packets) to the target node, the repeating node can append its packet to the end of the current packet.

  This function, along with the Ack-accelerated arbitration, is enabled in a Phy register named EAA. Please refer to the appropriate data sheet for further information.

- **Phy “pinging”**
  This provides a means of measuring the two-way travel time of packets transmitted between two nodes on the bus that are furthest from one another in terms of cable hops. This time can be used to optimize the “gap count” to minimize the idle bus time consumed by the subaction gap and the arbitration reset gap.

The Ping Packet is a firmware-generated packet that is explained in Section 4.3.4 of the IEEE 1394a-2000 standard. The min and max propagation formulas used to calculate the propagation delay are located in Annex E of the IEEE 1394a-2000 standard. Upon reception of a Ping Packet, the Phy automatically responds by sending a Self-ID packet out on the bus.

- **Priority arbitration**
  This allows a node that is transmitting asynchronous packets to arbitrate for the bus more than once during a fairness interval. There are limits imposed on how often a node can gain access to the bus in a fairness interval. These limits are defined by the FAIRNESS_BUDGET (also referred to as PRIORITY_BUDGET) register located in the CSR register space at offset 218h.

  The implementation of priority arbitration has no direct implications to the upgrade from the P11A to a P2x device. To implement priority arbitration the node's firmware will need to manage the appropriate CSR registers and set the proper bits in the link layer controller to enable this enhancement.

- **Port disable, suspend, and resume**
  This addition to the standard clearly defines these different port states and what actions must occur during these states. The definitions of these different port states are as follows:

  – **Disabled Port:** A port configured to neither transmit, receive, nor repeat Serial Bus signals.

    ♦ There are two ways to disable a port. First, the local link layer controller can directly set the disable bit located at base address 1000_b in the physical layer's (PHY) Page 0 (Port Status) Configuration register. Second, a port can become disabled by a remote command packet. The second way is a remote command packet may be sent from either the PHY's local link controller or by some other node. For more information on remote command packets, see section 4.3.4.4.4 in the IEEE 1394a-2000 standard.

  – **Suspended Port:** A connected port not operational for normal Serial Bus arbitration, but otherwise capable of detecting both a physical cable disconnection and received bias.

    ♦ A port becomes suspended when it receives a remote command packet that sets the port's suspend variable to one. The remote command packet may be sent from either the PHY's local link controller or by some other node. For more information on remote command packets, see section 4.3.4.4.4 in the IEEE 1394a-2000 standard.

  – **Resuming Port:** A previously suspended port that has observed bias or has been instructed to generate bias. In either case, the resuming port engages in a protocol with its connected peer PHY in order to re-establish normal operations and become active.

    ♦ Any of the following events can cause a suspended port to attempt to resume normal operations:

      ▪ Bias is detected and there is no fault condition.

      ▪ A resume packet is received or transmitted by the PHY. The resume packet may be sent from either the PHY's local link controller or by some other node. For more information on resume packets, see section 4.3.4.4.4 in the IEEE 1394a-2000 standard.

      ▪ A remote command packet that sets the resume variable to one is sent to the suspended port. The remote command packet may be sent from either the PHY's local link controller or by some other node. For more information on remote command packets, see section 4.3.4.4.4 in the IEEE 1394a-2000 standard.

      ▪ If the node is isolated and any disconnected (but enabled) port detects a new connection.

  For detailed information on Port disable, suspend, and resume protocols, please refer to section 3.9.5 in the IEEE 1394a-2000 standard.

3. REGISTER CONFIGURATIONS

This section describes the differences that exist between the P11A internal registers and the P2x internal registers.

3.1. P11A register configuration

The P11A has a register set that is defined by the IEEE 1394-1995 standard and is shown in Table 2.

Table 2. PDI1394P11A Internal Register configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Reserved		NP			
0011	AStat1		BSTAT1		Ch1	Con1	Reserved	
0100	AStat2		BSTAT2		Ch2	Con2	Reserved	
0101	AStat		BSTAT3		Ch3	Con3	Reserved	
0110	Loopint	CPSint	CPS	IR	Reserved			C
0111	Reserved				PC2	PC1	PC0	C
1000	Reserved							
1001	Reserved							ISBR

The Phy registers defined under the IEEE 1394-1995 standard have ten address locations that are 8 bits wide. For detailed explanations of each register and its function, please refer the the P11A datasheet and the IEEE 1394-1995 standard.

3.2. P2x Base Register configuration

The P2x has a register set that is defined by the IEEE 1394a-2000 standard, and is shown in Tables 3 through 6. Even though the P11A and the P2x devices share some base registers in common, the address locations and bit positions of these common functions may be different. Thus, when upgrading from a P11A to a P2x device firmware changes will need to be made to insure the proper value is being written to the proper location. Table 3 shows the base register set. Its primary purpose is to report or maintain the current node and bus configuration parameters.

Table 3. PDI1394P2x Base Register configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Rsvd	Num_Ports (0011b)			
0011	PHY_Speed (010b)			Rsvd	Delay (0001b)			
0100	LCtrl	C	Jitter (000)			Pwr_Class		
0101	RPIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_Select			Rsvd	Port Select			

3.3. Differences in Base Register configurations

The following list describes the differences that exist between the Base Registers of the P11A and the P2x devices. This comparison between register sets is to illustrate a basic difference between the P11A devices and the P2x family of devices. Since each device in the P2x family is different, minor deviations in the register sets may exist. When updating your firmware, please refer to the appropriate P2x data sheet to insure these deviations are dealt with properly.

- **Base Address 0000_b**
  These 8 bits are identical and will require no firmware changes to upgrade from a P11A to a P2x device.
- **Base Address 0001_b**
  These 8 bits are identical and will require no firmware changes to upgrade from a P11A to a P2x device.
- **Base Address 0010_b**
  The differences listed below are located in read only registers. The other bit positions not listed are identical in functionality.
  - **P11A:**
    - Bit positions 0–1: This register space defines the signaling speed of the PHY.
  - **P2x:**
    - Bit positions 0–2: This register space defines that the P2x family uses the extended register set.
- **Base Address 0011_b**
  - **P11A:**
    - Bit positions 0–1: This register space reports the line state of TPA1.
    - Bit positions 2–3: This register space reports the line state of TPB1.
    - Bit position 4: This register space reports if port 1 is a child or parent port.
    - Bit position 5: This register space reports if port 1 is connected or disconnected.
    - Bit positions 6–7: This register space is reserved.
  - **P2x:**
    - Bit positions 0–2: This register space reports the PHY speed capabilities.
    - Bit position 3: This is a reserved register space.
    - Bit positions 4–7: This register space reports the PHY repeater delay.
- **Base Address 0100_b**
  - **P11A:**
    - Bit positions 0–1: This register space reports the line state of TPA2.
    - Bit positions 2–3: This register space reports the line state of TPB2.
    - Bit position 4: This register space reports if port 2 is a child or parent port.
    - Bit position 5: This register space reports if port 2 is connected or disconnected.
    - Bit positions 6–7: This register space is reserved.
  - **P2x:**
    - Bit position 0: This register space reports the active status of the Link Layer Controller.
    - Bit position 1: This register space reports Bus manager/Isochronous Resource Manager Contender status.
    - Bit positions 2–4: This register space indicates the worst-case difference between the fastest and slowest repeater data delay.
    - Bit positions 5–7: This register space indicates the node’s power consumption and source characteristics.

- **Base Address 0101_b**
  - **P11A:**
    - Bit positions 0–1: This register space reports the line state of TPA3.
    - Bit positions 2–3: This register space reports the line state of TPB3.
    - Bit position 4: This register space reports if port 3 is a child or parent port.
    - Bit position 5: This register space reports if port 3 is connected or disconnected.
    - Bit positions 6–7: This register space is reserved.
  - **P2x:**
    - Bit position 0: This register space enables the port event interrupt bit to be set whenever resume operations begin.
    - Bit position 1: This register space instructs the PHY to initiate a short bus reset.
    - Bit position 2: This register space is set to a 1 when the arbitration controller times-out during tree-ID, which may indicate the bus is configured in a loop.
    - Bit position 3: This register space is an interrupt that flags when cable power may be too low.
    - Bit position 4: This register space is an interrupt that flags when a state time-out has occurred.
    - Bit position 5: This register space is an interrupt that flags when any port event has occurred assuming the appropriate Port Interrupt enable bits are set.
    - Bit position 6: This register space enables accelerated arbitration.
    - Bit position 7: This register space enables multi-speed concatenated packets.
- **Base Address 0110_b**
  - **P11A:**
    - Bit position 0: This register space is set to a 1 when the arbitration controller times-out during tree-ID, which may indicate the bus is configured in a loop.
    - Bit position 1: This register space is an interrupt that flags when cable voltage is too low.
    - Bit position 2: This register space is a redundant copy of the Cable Power Status register located at Base Address 0000_b bit position 7; its purpose is to expedite handling of the CPSint register.
    - Bit position 3: This register space indicates that this device initiated the previous bus reset.
    - Bit positions 4–6: This register space is reserved.
    - Bit position 7: This register is set if this node is contender for the bus manager or isochronous resource manager role.
  - **P2x:**
    - Bit positions 0–7: This register space is reserved.
- **Base Address 0111_b**
  - **P11A:**
    - Bit positions 0–3: This register space is reserved.
    - Bit position 4: This register space is where the Power Class 2 bit is stored.
    - Bit position 5: This register space is where the Power Class 1 bit is stored.
    - Bit position 6: This register space is where the Power Class 0 bit is stored.
    - Bit position 7: This register space is a redundant copy of the Contender register located at Base Address 0110_2 bit position 7.
  - **P2x:**
    - Bit positions 0–2: This register space is used to select the register page to use when accessing register addresses 8 through 15.
    - Bit position 3: This register space is reserved.
    - Bit positions 4–7: This register space is used to select the port when accessing per-port status or control.

- **Base Address 1000_b**
  - **P11A:**
    - Bit positions 0–7: This register space is reserved.
  - **P2x:**
    - Bit positions 0–7: This register space is located in the Page 0 Port Status registers, Page 1 Vendor ID registers, and Page 7 Vendor Dependent registers. Refer to the appropriate data sheet for details pertaining to these registers.
- **Base Address 1001_b**
  - **P11A:**
    - Bit positions 0–6: This register space is reserved.
    - Bit position 7: This register space instructs the P11A to initiate an arbitrated short bus reset.
  - **P2x:**
    - Bit positions 0–7: This register space is located in the Page 0 Port Status registers, Page 1 Vendor ID registers, and Page 7 Vendor Dependent registers. Refer to the appropriate data sheet for details pertaining to these registers.

3.3.1. Page 0 (Port Status) register

Table 4 shows the Page 0 Port Status registers, which provides access to configuration and status information for each of the ports. For an explanation of each register, please refer to the appropriate P2x data sheet; and for a detailed explanation of each function, please refer to the IEEE 1394a-2000 standard.

Table 4. PDI1394P2x Page 0 (Port Status) Register configuration

ADDRESS	BIT POSITION							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1000	AStat		BStat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

3.3.2. Page 1 Vendor ID register

Table 5 shows the Page 1 Vendor ID registers, which are used to identify the vendor/manufacturer and the compliance level of the device. The compliance level reports whether the chip is compliant to either the IEEE 1394-1995 standard or the IEEE 1394a-2000 standard. For an explanation of each register, please refer to the appropriate P2x data sheet; and for a detailed explanation of each function, please refer to the IEEE 1394a-2000 standard.

Table 5. PDI1394P2x Page 1 (Vendor ID) Register configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

3.3.3. Page 7 Vendor Dependent register

Table 6 shows the Page 7 Vendor Dependent registers, which provide access to configuration and status information used in manufacturing test and debug of the devices. There is one Rd/Wr register that is used to report the speed of the attached link layer controller. For an explanation of each register, please refer to the appropriate P2x data sheet; and for a detailed explanation of each function, please refer to the IEEE 1394a-2000 standard.

Table 6. PDI1394P2x Page 7 (Vendor Dependent) Register field descriptions

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Reserved						Link_Speed	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

4. TYPICAL PHY SCHEMATIC DESIGN

This section highlights a P11A design and a P21 design. This section is described as typical because the represented designs can be used in many applications.

4.1. P11A design

Figure 1 represents a typical P11A PHY design. From a schematic point of view, a P11A design is not much different from a P2x design. Many of the external components required on the P11A are exactly the same on a P2x design. The biggest differences between a P11A design and a P2x design are:

1. The P11A is a 200 Mb/s device, and the P2x is a 400 Mb/s device. Because of the higher frequency, more care needs to be taken in laying out the traces between the P2x PHY pins and the connectors. See comments in Section 4.2., “P2x Design”.
2. Because the P11A is a 200 Mb/s device, it has four data lines (D0–D3) to interface to the Link Layer Controller. Because of their higher data rate, the P2x devices have eight data lines (D0–D7) that interface to the Link Layer Controller.
3. The P11A has a pin called “FILTER” that is tied to ground through a 0.1 μF capacitor. This pin is used in a lag-lead filter for a PLL frequency multiplier. The P2x devices do not need this external capacitor.
4. The P11A has two test mode pins called TESTM1 and TESTM2. These pins are used for two reasons. First, they are used for manufacturing to enable production testing of the devices. Secondly, they can be used to enable the ISBR (Arbitrated [short] bus reset). Refer to the P11A data sheet for details on configuring these pins. The P2x devices have two similar pins called TEST0 and TEST1. These pins are exclusively used for manufacturing testing of these devices, except for the P23 and P25. Refer to the appropriate data sheet for further details.

Transitioning from the Philips Semiconductors PDI1394P11A to the PDI1394P2x family

AN2455

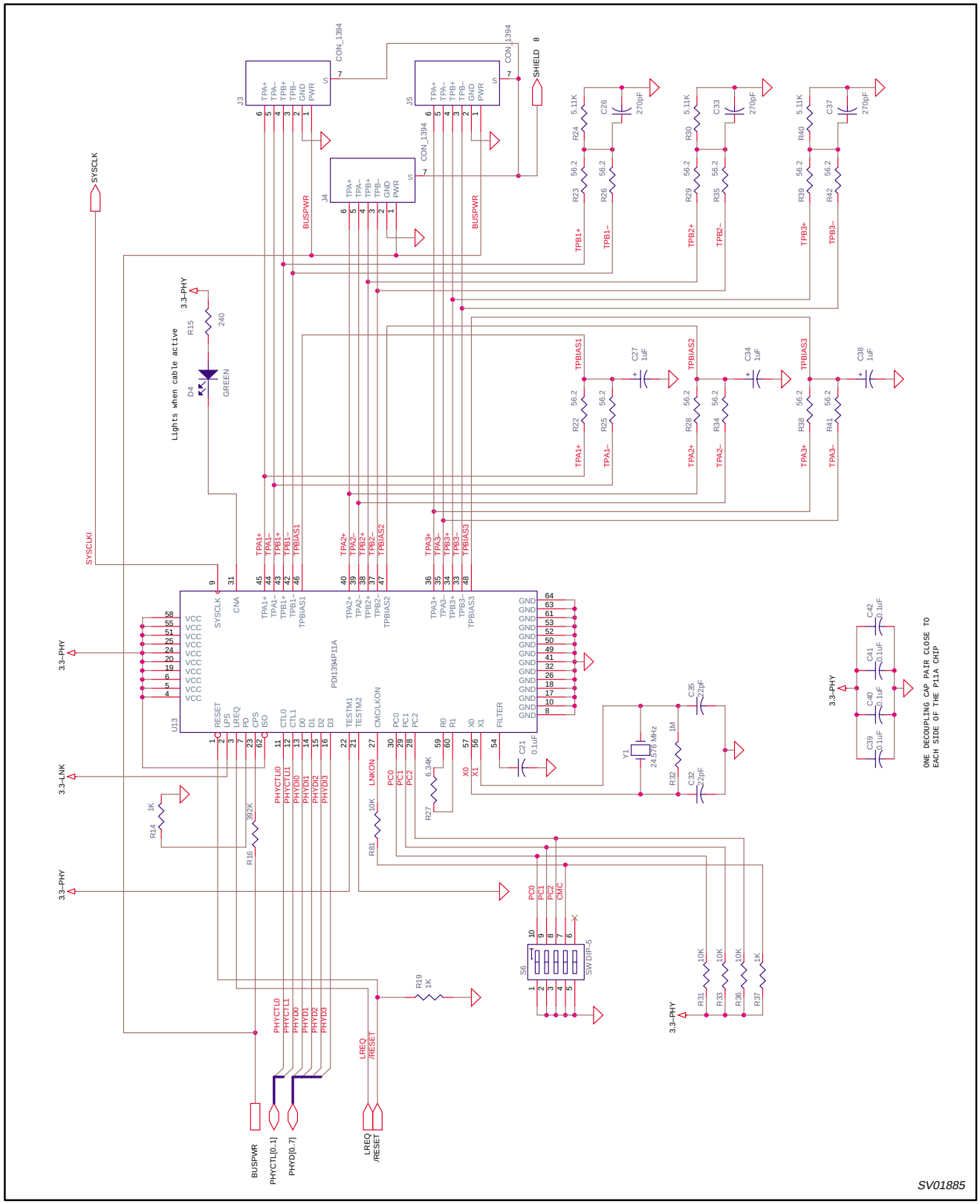

Figure 1. Typical P11A design

4.2. P2x design

Figure 2 shows a typical P21 schematic design that has many things in common with all P2x designs. This design does not implement Galvanic Isolation. For more information on how and why to implement Galvanic Isolation, please refer to Philips Semiconductors' application note AN2452, titled *'IEEE 1394 bus node galvanic isolation and power supply design'*.

4.2.1. P21 common elements to all P2x designs

The common design elements are referred to as common because they are implemented the same, regardless of which P2x PHY is chosen. All of the external components required for the PHY will be exactly the same for each member of the P2x family (unless otherwise noted).

All of the PHY/Link interface signals are implemented the same, and require no external components except for LPS and C/LKON. The interface signals are ISO, SYSCLK, LREQ, D0–D7, CLT0, CLT1, C/LKON, and LPS. For the LPS and C/LKON signals, please refer to the appropriate data sheet for our recommendations on proper design of these signals.

The port designs are also the same for all of the P2x devices. Some PHYs have more ports than others, but the external components required for each port are exactly the same. These are high speed ports (up to 400 Mb/s), so care should be taken to insure that the length of the TPAn+, TPAn–, TPBn+, and TPBn– traces are as close to the same length as possible to minimize skew. It is also recommended that the 56.2 Ω resistors be placed as close to the PHY pins as possible.

All of the P2x devices also use the same crystal design. Refer to the appropriate data sheet for specifications and our recommended design.

We recommend that the Link Layer Controller (LLC) and the PHY share the same $\overline{\text{RESET}}$ signal. If the design uses both a LLC and a PHY, it is recommended that external logic be used to control the timing of the $\overline{\text{RESET}}$ line. If the PHY is going to be implemented as a repeater only (no LLC), then a 0.1 μF capacitor should be connected between the PHY $\overline{\text{RESET}}$ line and GND to insure minimum timing requirements are met. Refer to the appropriate data sheet for design recommendations and timing requirements.

The Power Class programming pins are the same on all P2x devices. These pins are used to report the default value of the power class of your node. Each data sheet has a table that explains the encoding scheme of these pins.

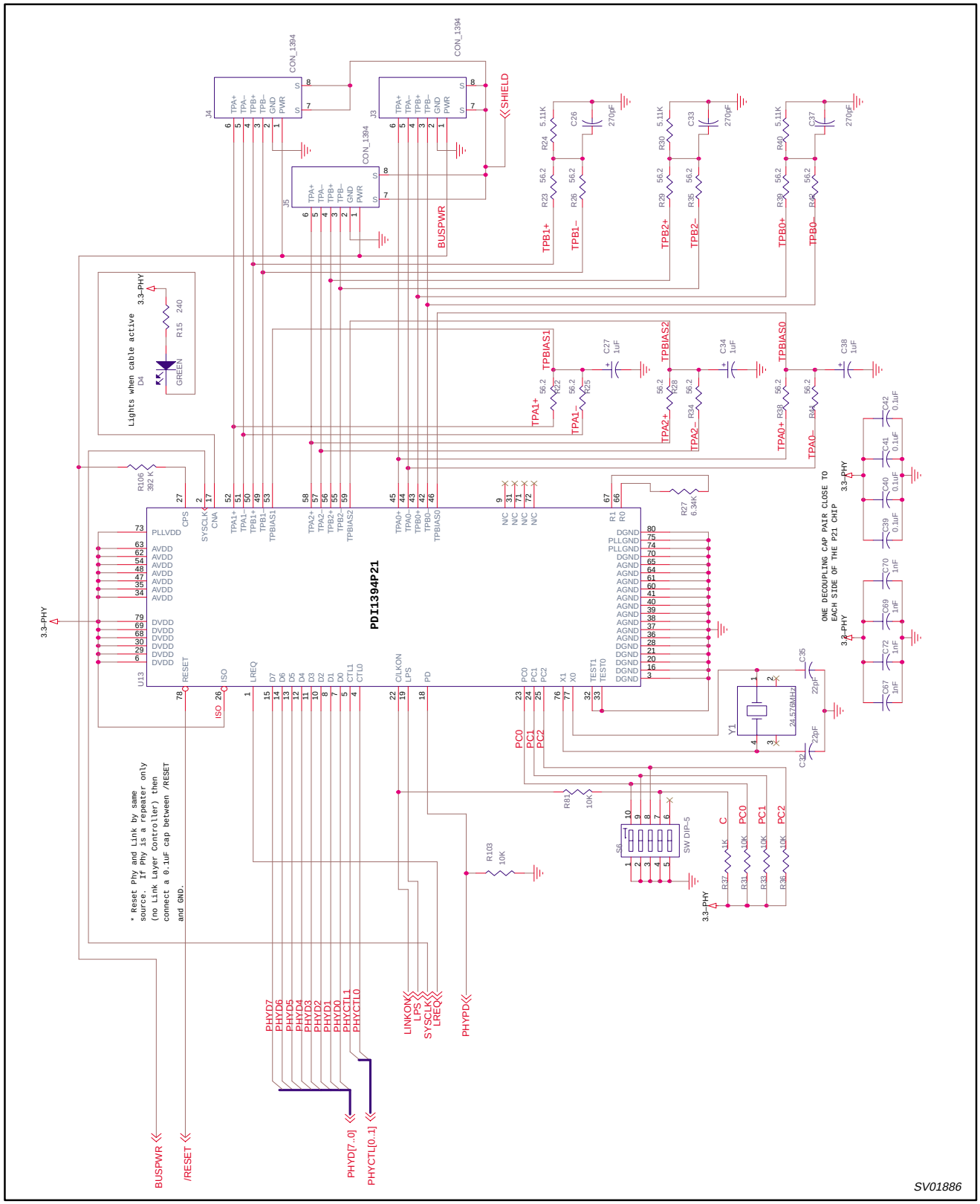

Figure 2. Typical P21 design

5. CONTACT INFORMATION

In case of any questions or suggestions regarding this application note or any other related 1394 issues, please feel free to contact the Philips 1394 Applications and Marketing group at **1394@abq.sc.philips.com**. For information on Philips Semiconductors' 1394 chipsets and tools, please visit our web site at **www.semiconductors.philips.com/1394**.

6. REFERENCES

- IEEE Std. 1394-1995
- IEEE Std. 1394a-2000
- PDI1394P11A data sheet
- PDI1394P21 data sheet
- PDI1394P22 data sheet
- PDI1394P23 data sheet
- PDI1394P24 data sheet
- PDI1394P25 data sheet
- *Fire Wire System Architecture*, Second Edition; Don Anderson; MindShare, Inc.; 1999; ISBN 0-201-48535-4.
- 1394 Trade Association Website: **http://www.1394ta.org/**

NOTES

Transitioning from the Philips Semiconductors PDI1394P11A to the PDI1394P2x family

AN2455

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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